PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Mitsutoshi MIYASAKA

Rule 53(b) Divisional of
Application No.: 09/400,303

Filed: March 19, 2002 Docket No.: 038839.02

For: A METHOD FOR FORMING CRYSTALLINE SEMICONDUCTOR LAYERS, A METHOD FOR FABRICATING THIN FILM TRANSISTORS, AND A METHOD FOR FABRICATING SOLAR CELLS AND ACTIVE MATRIX LIQUID CRYSTAL DEVICES

PRELIMINARY AMENDMENT

Assistant Commissioner of Patents
Washington, D. C. 20231

Sir:

Prior to initial examination, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Page 1, line 1, delete in its entirety.

Page 1, between lines 5 and 6, insert the following centered heading:

BACKGROUND OF THE INVENTION

Page 1, line 6:

Field of The Invention

Page 1, line 12:

Description of the Related Art

Page 3, line 25:

SUMMARY OF THE INVENTION

Page 20, between lines 11 and 12, insert the following centered heading and succeeding paragraphs:

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1 (a) through (d) show cross-sectional views of the steps in the TFT fabrication process of the present invention.

Figure 2(a) is a schematic diagram showing the essential components of the RTA unit used for the second annealing step in the present invention.

Figure 2(b) explains the annealing state during the second annealing step.

Figure 2(c) shows the temperature profile in the RTA unit.

Figure 3 shows the relationship between the annealing temperature, the annealing time, and the resulting effect (TFT mobility) for the second annealing step in the present invention.

Figure 4 shows the relationship between the time factor β during the second annealing step in the present invention and the effect (TFT mobility) of the second annealing step.

Figure 5 shows the relationship between the time factor β and the resulting effect (variation in TFT mobility) for the second annealing step in the present invention.

Figures 6 (a) through (d) schematically show in cross-section the process steps of one portion of the fabrication procedure for solar cells according to the present invention.

Figures 7 (a) through (d) schematically show in cross-section the process steps of one portion of the fabrication procedure for solar cells according to the present invention.

Figures 8 (a) through (d) schematically show in cross-section the process steps of one portion of the fabrication procedure for solar cells according to the present invention.

Figures 9 (a) through (c) are schematic diagrams of the essential components of the annealing unit used in the first annealing step of the present invention.

Figures 10 (a) through (d) schematically show in cross-section the process steps of one portion of the fabrication procedure for solar cells according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Page 49, line 14 to page 50, line 10, delete in its entirety.

Page 50, between lines 18 and 19, insert the following centered heading:

EXAMPLES

Page 66, line 35 to page 67, line 26:

Then a tantalum (Ta) thin film, which becomes gate electrode 15, is deposited by means of sputtering. The substrate temperature at the time of sputtering is 150°C, and the film thickness is 500 nm. Patterning is carried out after the tantalum thin film, which is to become the gate electrode, is deposited. This is followed by implantation of impurity ions in the semiconductor layer and formation of source and drain regions 16 and channel region 17 (FIG. 1(c)). In this example, because CMOS TFTs are being formed, NMOS TFTs and PMOS TFTs are formed on a single substrate. The PMOS TFTs are covered with polyimide during formation of the sources and drains of the NMOS TFTs; conversely, the NMOS TFTs are covered with polyimide during formation of the sources and drains of the PMOS TFTs, thereby making CMOS TFTs. At this time, the gate electrode serves as a mask for ion implantation, and the channel becomes a self-aligned structure that is formed only below the gate electrode. Impurity ion implantation is carried out using a non-mass separating ion implanter and phosphine (PH_3) or diborane (B_2H_6) diluted by hydrogen to a concentration of approximately 5% as the source gas. For NMOS, the total ion implantation dose, including ions such as PH_3^+ and H_2^+, is 1×10^{16} cm^{-2} and the phosphorous atom concentration in the source and drain regions is approximately 3×10^{20} cm^{-3}. Similarly, for PMOS, the total ion implantation dose, including ions such as $B_2H_6^+$ and H_2^+, is also 1×10^{16} cm^{-2} and the boron

atom concentration in the source and drain regions is approximately 3 x 10^{20} cm^{-3}. The substrate temperature at the time of ion implantation is 250°C.

Page 67, line 27 to page 68, line 3:

Next, interlevel insulator layer 18, comprised of a silicon oxide film, is formed by means of PECVD using TEOS. The substrate surface temperature during interlevel insulator layer deposition is 350°C., and the layer thickness is 500 nm. After the interlevel insulator layer is formed, thermal annealing is performed for 1 hour at 350°C. in an oxygen atmosphere to achieve activation of implanted ions and densification of the interlevel insulator layer. Contact holes are then opened to the source and drain regions, and aluminum (Al) is deposited by means of sputtering. The substrate temperature during sputtering is 150°C., and the film thickness is 500 nm. Patterning is carried out on the aluminum thin film source and drain electrodes 10 and interconnects to complete the thin film semiconductor device (FIG. 1(d)).

Page 68, lines 4-11:

In this example, with the goal of investigating the transistor performance and the nonuniformity within a single substrate, 50 transistors uniformly fabricated over a large substrate and having channel lengths L=5 μm and widths W=5 μm were measured. The results are as shown below. The on current is defined at $|V_{ds}|$ =4 V and $|V_{gs}|$ =10 V while the off current is defined at $|V_{ds}|$ =4 V and $|V_{gs}|$ =0 V.

Page 71, line 4, delete in its entirety.

REMARKS

Claims 1-8 are pending. By this Preliminary Amendment, the specification is amended to conform the application to U.S. practice. No new matter is added. Early and favorable examination of the application is respectfully requested.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Joel S. Armstrong
Registration No. 36,430

JAO:JSA

Attachment:
Appendix

Date: March 19, 2002

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

APPENDIX

Changes to Specification:

Page 1, line 1, delete in its entirety.

Page 1, between lines 5 and 6, insert the following centered heading:

BACKGROUND OF THE INVENTION

Page 1, line 6:

Field of ~~Technology~~ the Invention

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Figure 3 shows the relationship between the annealing temperature, the annealing time, and the resulting effect (TFT mobility) for the second annealing step in the present invention.

Figure 4 shows the relationship between the time factor β during the second annealing step in the present invention and the effect (TFT mobility) of the second annealing step.

Figure 5 shows the relationship between the time factor β and the resulting effect (variation in TFT mobility) for the second annealing step in the present invention.

Figures 6 (a) through (d) schematically show in cross-section the process steps of one portion of the fabrication procedure for solar cells according to the present invention.

Figures 7 (a) through (d) schematically show in cross-section the process steps of one portion of the fabrication procedure for solar cells according to the present invention.

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Figures 9 (a) through (c) are schematic diagrams of the essential components of the annealing unit used in the first annealing step of the present invention.

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Next, interlevel insulator layer ~~109~~ 18, comprised of a silicon oxide film, is formed by means of PECVD using TEOS. The substrate surface temperature during interlevel insulator layer deposition is 350°C., and the layer thickness is 500 nm. After the interlevel insulator layer is formed, thermal annealing is performed for 1 hour at 350°C. in an oxygen atmosphere to achieve activation of implanted ions and densification of the interlevel insulator layer. Contact holes are then opened to the source and drain regions, and aluminum (Al) is deposited by means of sputtering. The substrate temperature during sputtering is 150°C., and the film thickness is 500 nm. Patterning is carried out on the aluminum thin film source and drain electrodes ~~110~~ 10 and interconnects to complete the thin film semiconductor device (FIG. 1(d)).

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